REMARKS/ARGUMENTS

1. Priority:

The declaration incorrectly refers to foreign priority based on Taiwan application 60/440,046. However, it is believed that the priority being claimed is the US provisional application 60/440,046. If this is the case, the applicants are required to submit a substitute declaration or oath to correct the deficiencies set forth above.

Response:

The applicants are submitting a supplemental application data sheet along with this amendment to correct the incorrect priority claim. According to MPEP 601.05, the supplemental application data sheet will govern over the declaration when there is inconsistent information in the priority claim. Therefore, the claim of provisional priority based on US provisional application 60/440,046 should now be clear on the record.

2. Objection to the specification:

The disclosure is objected to due to informalities.

Response:

The specification has been amended to correct the two informalities pointed out by the examiner. Acceptance of the corrected specification is respectfully requested.

3. Rejection of claims 1, 2, 6, 7, 9-13, 17, 18, 20-29, 30-32, 35-37, and 40 under 35 U.S.C. 102(e):

Claims 1, 2, 6, 7, 9-13, 17, 18, 20-29, 30-32, 35-37, and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Hook et al. (US 6,564,304, hereinafter referred to as "Van Hook") for reasons of record.

Response:

The applicant would like to point out how the claims are patentably distinguished from Van Hook.

Claim 1 contains the following limitations that are not taught in the prior art:

- "the memory controller comprising a request queue".

Instead, Van Hook teaches "Each memory master M0-M4 has an associated request queue RQ0-RQ4 respectively" [col. 4, line 62] and "Memory controller 105 is coupled with each of request queues RQ0-RQ4 and orders the requests in RQ0-RQ4" [col. 4 line 65].

Therefore, Van Hook teaches that each memory master has its own request queue and the request queue is coupled to the memory controller. Van Hook does not teach that the memory controller comprises a request queue, as is claimed.

- "a latency monitoring unit electrically connected to the request queue".

Van Hook teaches "The memory master also provides latency requirement information about itself in the request queue" [col. 4, line 39].

Thus, Van Hook teaches that the latency information is provided in the request queue. However, Van Hook does not teach that a latency monitoring unit electrically connected to the request queue, as is recited in claim 1.

- (b) using the latency monitoring unit to record a plurality of latency values, the latency value respectively corresponding to the access requests stored in the request queue

Van Hook teaches "The memory master also provides latency requirement information about itself in the request queue" [col. 4, line 39].

Therefore, Van Hook teaches that the latency information is provided in the request queue. Van Hook does not teach that the latency values are recorded in latency monitoring unit which is electrically connected to the request queue

- (c) using the memory controller to receive a first access request and add the first access request to the request queue with an associated queue priority according to the latency values associated with the access requests already stored in the request queue.

Van Hook teaches "A bypass path 104 is provided directly to the sort queue so that high priority request can be handled out of turn and satisfied within latency requirements" [col. 5, line 15].

In other words, Van Hook teaches that a bypassing path is provided to satisfy the latency requirements of the high priority request. Van Hook does not teach that the latency values of the access request already stored in the request queue are taken into consideration when ordering a new added request.

- (d) using the memory controller to sequentially access the memory device according to the associated queue priorities of the access requests stored in the request queue.

Van Hook teaches "After sorting the system performs the requests in the sorted order **unless a higher priority request occurs**" [col. 5, line 64].

Thus Van Hook teaches that if a higher priority request occurs, the request accessed is terminated. However, in the instant application, request accessed will not be terminated in this situation.

Claim 2 claims that access requests for the same page of memory are put together in the request queue. However, Van Hook teaches in col. 5, line 48 that "reads and writes are reordered at step 201. The reordering involves grouping reads

together with reads and writes together with writes as much as possible. Then page accesses **within a memory bank are grouped together** and sorted at step 202". That is, Van Hook teaches that reads and writes are respectively grouped together, and that pages within a memory bank are grouped together. Van Hook does not teach that the requests with same page are put together, as is claimed.

Claim 12 contains the following limitations that are not taught in the prior art:

- (c) receiving a first access request and adding the first access request to the request queue with an associated queue priority according to latency values associated with the access requests already stored in the request queue.

Van hook teaches in col. 5, line 15 that "A bypass path 104 is provided directly to the sort queue so that high priority request can be handled out of turn and satisfied within latency requirements." That is, Van Hook teaches that a bypassing path is provided to satisfy the latency requirements of the high priority request. Van Hook does not teach that the latency values of the access request already stored in the request queue are taken into consideration when ordering a new added request.

- (d) sequentially access the memory device according to the associated queue priorities of the access requests stored in the request queue.

Van Hook teaches in col. 5, line 64 "After sorting the system performs the requests in the sorted order **unless a higher priority request occurs**". Thus, Van Hook teaches that if a higher priority request occurs, the request accessed is terminated. However, in the instant application, request accessed will not be terminated.

Claims **13, 30, and 36** each claim that access requests for the same page of memory are put together in the request queue. However, Van Hook teaches in col. 5,

line 48 that "reads and writes are reordered at step 201. The reordering involves grouping reads together with reads and writes together with writes as much as possible. Then page accesses **within a memory bank are grouped together** and sorted at step 202". That is, Van Hook teaches that reads and writes are respectively grouped together, and that pages within a memory bank are grouped together. Van Hook does not teach that the requests with same page are put together, as is claimed.

Claim 23 contains the following limitations that are not taught in the prior art:

- A latency monitoring unit electrically connected to the request queue for recording a plurality of latency values, the latency values respectively corresponding to the access requests stored in the request queue.

On the other hand, Van Hook teaches in col. 4, line 39 "The memory master also provides latency requirement information about itself **in the request queue**".

Van Hook teaches that the latency information is provided in the request queue. However, Van Hook does not teach that the latency values are recorded in latency monitoring unit which is electrically connected to the request queue.

- Wherein the memory controller is sequentially accessed according to the associated queue priorities of the access requests stored in the request queue.

Van Hook teaches in col. 5 line 64 "After sorting the system performs the requests in the sorted order **unless a higher priority request occurs**".

That is, Van Hook teaches that if a higher priority request occurs, the request accessed is terminated. However, in the instant application, request accessed will not be terminated.

Claim 24 claims a page/bank comparing unit electrically connected to the reorder decision-marking unit and the request queue comparing the pages of memory

that the access requests correspond to, so as to group access requests for the same page of memory together. On the other hand, Van Hook teaches in col. 5, line 49 "The reordering involves grouping reads together with reads and writes together with writes as much as possible. Then page accesses **within a memory bank are grouped together** and sorted at step 202". Therefore, Van Hook does not teach that a page/bank comparing unit is electrically connected to the reorder decision-marking unit.

Claim 25 claims a latency control unit for comparing latency values to a maximum value. As cited by the examiner, Van Hook teaches "The memory controller uses the queue and page break decisions to provide appropriate reordering of the requests from all of the request queues for efficient page and bank access while considering latency requirements" [col. 3 line 66] and "A bypass path 104 is provided directly to the sort queue so that high priority request can be handled out of turn and satisfied within latency requirements" [col. 5 line 15].

Van Hook considers latency requirements for high priority requests, however the latency values of the already stored requests in the request queue are considered in the instant application. In the instant application, if a new added request will make the latency value of an already stored request in the request queue exceed a maximum allowance value, the reorder will not be made. On the other hand, Van Hook does not teach that the reorder will not be made.

In addition to the arguments given above, claims 2-11, 13-22, 24-29, 31-35, and 37-40 are dependent on independent claims 1, 12, 23, 30, and 36, respectively, and should be allowed if their respective independent claims are allowed. Reconsideration of claims 1-40 is therefore respectfully requested.

In view of the claim amendments and the reasons given above, the applicants

respectfully request that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Winston Hsu Date: November 15, 2005

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
10 Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)